INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/96	Serial No. 10/551,891
	Applicant(s) VORBACH	
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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	3,753,008	August 14, 1973	Guarnaschelli			
	4,594,682	June 10, 1986	Drimak			
	5,996,048	November 30, 1999	Cherabuddi et al.			
	6,260,114	July 10, 2001	Schug			
	6,496,902	December 17, 2002	Faanes et al.			
	2002/0073282	June 13, 2002	Chauvel et al.			
	2003/0070059	April 10, 2003	Dally et al.			
	2005/0091468	April 28, 2005	Morita et al.			
	2008/0313383	December 18, 2008	Morita et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	ARM Limited, "ARM Architecture Reference Manual," December 6, 2000, pp. A10-6-A10-7.
	Li, Zhiyuan, et al., "Configuration prefetching techniques for partial reconfigurable coprocessor with relocation and defragmentation," International Symposium on Field Programmable Gate Arrays, February 1, 2002, pp. 187-195.
	Melvin, Stephen et al., "Hardware Support for Large Atomic Units in Dynamically Scheduled Machines," Computer Science Division, University of California, Berkeley, IEEE (1988), pp. 60-63.
	Roterberg, Eric., et al., "Trace Cache: a Low Latency Approach to High Bandwidth Instruction Fetching," Proceedings of the 29th Annual Internatinoal Symposium on Michoarchitecture, Paris, France, IEEE (1996), 12 pages.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.